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EXAMINER	
JOHNSON, BRIAN P	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/801,942	MOORE, CHARLES H.	
	Examiner	Art Unit	
	BRIAN P. JOHNSON	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26,29,30,34-36 and 40-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26,29,30,34-36 and 40-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26, 29-30, 34-36, and 40-59 have been examined.

2. Acknowledgement of papers filed: remarks and claim amendments on 19 December 2009. These papers filed have been placed on record.

Claim Objections

3. Objection is withdrawn.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Rejection is withdrawn.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-14, 16-21, 23-26, 30, 34, 40-42, 45-55, and 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii in view of Pechanek (U.S.

Patent No. 6,023,753 -- herein Penachek1) in further view of Schreiber (U.S. Patent No. 6,507,947).

7. Regarding claim 1, Fujii discloses a computer array, comprising: a plurality of computers and a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of computers ([0072]); and wherein, at least some of the computers are assigned a communication from that assigned to the other computers ([0008]).

Fujii fails to disclose that the computers are integrated on a unitary substrate.

Pechanek1 discloses a plurality of computers on an array on an integrated circuit (col 2 lines 24-27).

Fujii would have been motivated to utilize the teachings of Pechanek1 for the reasons outlined in Pechanek1 col 2:

"Since the total number of wires in a torus connected computer can be significant, the interconnections may consume a great deal of valuable integrated circuit "real estate", or the area of the chip taken up. Additionally, the PE interconnection paths quite frequently cross over one another complicated the IC layout process and possibly introducing noise to the communication lines through crosstalk. Furthermore, the length of wraparound links, which connect PEs at the North and South and at the East and West extremes of the array, increase with increasing array size. The increased length increases each communication line's capacitance, thereby reducing the line's maximum bit rate and introducing additional noise to the lines."

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Fujii and incorporate the integrated substrate of Pechanek1.

Fujii fails to disclose a plurality of computers including read-only memory and random access memory for holding instructions and data.

Schreiber discloses the limitations that Fujii lacks (col 32 lines 1-24).

Fujii would have been motivated to have individual memory components for each individual processing element to easy access to instructions/data for execution.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Fujii and incorporate the individual RAM and ROM elements, as in Schreiber.

8. Regarding claim 2, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: each of the computers is assigned a task different from that of the other computers [0008])

9. Regarding claim 3, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: at least some of the computers are configured for specific input functions ([0008]), whereby the computers configured for specific input functions can receive data from an external device ([0003]) and communicate the received data to other computers of the array ([0072]).

10. Regarding claim 4, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: at least some of the computers are configured for specific output functions ([0008]), whereby the computers configured for specific output functions can receive data from other computers in the array ([0072]) and communicate the received data to an external device ([0057]).

11. Regarding claim 6, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: communication between the computers is via a plurality of parallel data lines (fig. 2, 4A, 11, and 12).

12. Regarding claim 7, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: each of the computers is hard wired to communicate with at least three of the plurality of computers (fig. 11).

13. Regarding claim 8, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: the quantity of the computers is 25 (fig. 3).

14. Regarding claim 9, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: the computers arc physically arraigned in a 5 by 5 array (fig. 3).

15. Regarding claim 10, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: at least some of the computers are physic, ally arrayed in a 4 by 6 array (fig. 3).

16. Regarding claim 11, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: the quantity of the computers along each side of the array is an even number (fig. 3).

17. Regarding claim 12, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: at least one, but not all, of the computers is in direct communication with an external memory source ([0053], [0057], and fig. 5).

18. Regarding claim 13, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: at least one of the computers communicates data from an external memory source to at least some of the plurality of computers ([0072]).

19. Regarding claim 14, Fujii/Pechanek1/Schreiber discloses a method for performing a computerized job, comprising: providing a plurality of computers integrated in a unitary substrate (Penchanek1 col 2 lines 24-27) and interconnected via discrete sets of data lines, each set of data lines being dedicated to a particular pair of the computers ([0072]); assigning a different task to at least some of the computers; and executing the tasks on the assigned computers ([0008]); and wherein each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24).

20. Regarding claim 16, Fujii/Pechanek1/Schreiber discloses the method of claim 14, wherein at least one of the computers is assigned to communication with an external random access memory (Schreiber col 32 lines 1-24).

21.

22. Regarding claim 17, Fujii/Pechanek1/Schreiber discloses the method of claim 14, wherein: at least one of the computers accomplishes an input/output function by transferring information between another of the computers and an external device ([0072]).

23. Regarding claim 18, Fujii/Pechanek1/Schreiber discloses the method of claim 14, wherein: one of the computers routes assignments to the remainder of the computers ([0057]-[0058]).

24. Regarding claim 19, Fujii/Pechanek1/Schreiber discloses a computer array, comprising: a plurality of computers on an integrated circuit chip (Pechanek1 col 2 lines 24-27) each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24); and a plurality of data connections between the computers, each of the data connections being directly accessible to no more than two of the computers ([0072]), wherein at least some of the computers are programmed to perform different tasks ([0008]).

25. Regarding claim 20, Fujii/Pechanek1/Schreiber discloses the computer array of claim 19, wherein: the different functions work together to accomplish a task ([0002]-[0006]).

26. Regarding claim 21, Fujii/Pechanek1/Schreiber discloses the computer array of claim 19, wherein: each of the functions is programmed into the respective computers when the computer array is initialized ([0002]-[0006] and [0057]-[0058]).

27. Regarding claim 23, Fujii/Pechanek1/Schreiber discloses a method for accomplishing a task using a plurality of computers, comprising: providing the plurality of computers on an integrated substrate (Pechanek1 col 2 lines 24-27) and interconnected by data lines, some of the data lines being accessible to no more than two of the computers ([0072]); dividing a task into operational components and assigning each of the operational components to one of the computers; programming at least some of the computers to accomplish each of the operational components; and executing the operational components on the assigned computers ([0008]); and wherein each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24).

28. Regarding claim 24, Fujii/Pechanek1/Schreiber discloses the method for accomplishing a task of claim 23, wherein: the operational components are operations used in accomplishing functions of a global positioning system receiver.

Note that Fujii/Pechanek1/Schreiber discloses this limitation in that it is capable of accomplishing functions of most any computing system.

29. Regarding claim 25, Fujii/Pechanek1/Schreiber discloses the method for accomplishing a task of claim 23, wherein: before the task is begun, programming the computers to accomplish each of the operational components ([0008]).

30. Regarding claim 26, Fujii/Pechanek1/Schreiber discloses the method for accomplishing a task of claim 23, wherein: the computers are arranged in a computer array ([00072]).

31. Regarding claim 30, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: each at least one of the read-only memory and the random access memory in each of the computers is dedicated memory ([0050]; Schreiber col 32 lines 1-24)

32. Regarding claim 34, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: each of the computers is an independently functioning computer ([0008]).

33. Regarding claim 40, Fujii/Pechanek1/Schreiber discloses the computer array of claim 1, wherein: the computers are the same with respect to at least one of structure, circuitry, layout, and operational characteristics (fig. 5).

34. Regarding claim 41, Fujii/Pechanek1/Schreiber discloses the computer array of claim 40, wherein: a first one of the computers is directly adjacent to a second one of the computers (fig. 5); and the first one of the computers is a mirror image of the second one of the computers (fig. 11)

35. Regarding claim 42, Fujii/Pechanek1/Schreiber discloses a computer array, comprising: a plurality of computers integrated on a substrate (Pechanek1 col 2 lines 25-27), each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24); and a plurality of data paths connecting the computers ([0072]), and wherein at lest some of the computers are assigned a task different from that assigned to the other computers ([0008]) and at least some of the computers include dedicated memory for the exclusive use of an associated one of the computers ([0050])

36. Regarding claim 45, Fujii/Pechanek1/Schreiber discloses a computer array of claim 1, wherein: the plurality of computers includes at least twenty-four computers (fig. 3).

37. Regarding claim 46, Fujii/Pechanek1/Schreiber discloses a computer array of claim 1, wherein: data communicated within the array from a first one of the computers

to a second one of the computers must necessarily pass through at least one of the other computers (fig. 11 top left to bottom right, for example).

38. Regarding claim 47, Fujii/Pechanek1/Schreiber discloses a computer array of claim 46, wherein: data communicated within the array from the first one of the computers to the second one of the computers must necessarily pass through at least two of the other computers (fig. 11 top left to bottom right, for example).

39. Regarding claim 48, Fujii/Pechanek1/Schreiber discloses a computer array of claim 1, wherein: at least some of the computers are programmed to function as an input and/or output interface between an external device and other computers of the array ([0050]).

40. Regarding claim 49, Fujii/Pechanek1/Schreiber discloses a computer array of claim 1, wherein: the computer array is a homogeneous array (fig. 5).

41. Regarding claim 50, Fujii/Pechanek1/Schreiber discloses a computer array, comprising: a plurality of computers each hard wired to communicate with at least three of the plurality of computers (fig. 11); and a plurality of data paths connecting the computers, each of the data paths being dedicated to an adjacent pair of the computers ([0072]); and wherein, at least some of the computers are assigned a task different from

that assigned to the other computers ([0008]), each of the plurality of computers is integrated on a unitary substrate (Pechanek1 col 2 lines 25-27).

42. Regarding claim 51, Fujii/Pechanek1/Schreiber discloses the computer array of claim 50, wherein: every one of the computers of the array is hard wired to communicate with at least three of the plurality of computers ([0072]).

43. Regarding claim 52, Fujii/Pechanek1/Schreiber discloses the computer array of claim 50, wherein: every one of the computers is hard wired to at least three data paths ([0072]); and each of the three data paths is coupled to a neighboring one of the computers (fig. 11) or provides a connection to an external device.

44. Regarding claim 53, Fujii/Pechanek1/Schreiber discloses a computer array, comprising: a plurality of computers each hard wired to communicate with at least three of the plurality of computers ([0072] and fig. 11); and a plurality of data paths connecting the computers, at least some of the data paths being connected to no more than two of the computers ([0072]); and wherein, at least some of the computers arc assigned a task different from that assigned to the other computers ([0008]); and wherein each of the plurality of computers is integrated on a unitary substrate (Pechanek1 col 2 lines 25-27); and each of the plurality of computers includes read-only memory for storing data instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24).

45. Regarding claim 54, Fujii/Pechanek1/Schreiber discloses the computer army of claim 53, wherein: every one of the computers of the array is hard wired to communicate with at least three of the plurality of computers ([0072] and fig. 11).

46. Regarding claim 55, Fujii/Pechanek1/Schreiber discloses the computer array of claim 53, wherein: every one of the computers is hard wired to at least three data paths; and each of the three data paths is coupled to a neighboring one of the computers or provides a connection to an external device ([0072]).

47. Regarding claim 57, Fujii/Pechanek1/Schreiber discloses a a computer array, comprising: a plurality of computers integrated into a unitary substrate (Pechanek1 col 2 lines 25-27), each of the plurality of computers including read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24); and a plurality of data paths connecting the computers, the data paths being physical, point-to-point links between associated pairs of computers ([0072]), and wherein, at last some of the computers are assigned a task different from that assigned to the other computers ([0008]).

48. Regarding claim 58, Fujii/Schreiber discloses a computer array, comprising: a plurality of independently functioning computers arranged in a matrix ([0008]), each of

said plurality of computers having at least two nearest neighbor computers (fig. 11); and a plurality of sets of interconnecting dedicated data lines ([0072]), each individual set of said plurality of sets of data lines being disposed between an individual computer and one of its nearest neighbor computers of said plurality of computers (fig. 11) or between said individual computer and an external device, some of said plurality of sets of data lines each being connected to no more than two of said plurality of computers ([0072]); thereby enabling execution era plurality of tasks by said plurality of computers, the execution of some of said tasks being different from the execution of others of said tasks ([0008]), and wherein each of said plurality of computers communicates with at least three others of said plurality of computers within said matrix (fig. 11); and each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24).

49. Regarding claim 59, Fujii/Schreiber discloses a computer array, comprising: a plurality of independently functioning computers arranged in a matrix ([0008]), each of said plurality of computers having at least two nearest neighbor computers (fig. 11); and a plurality of sots of interconnecting dedicated data lines ([0072]), each individual set of said plurality of sets of data lines being disposed between an individual computer and one of its nearest neighbor computers of said plurality of computers; thereby enabling execution of a plurality of tasks by said plurality of computers ([0008]), the execution of some of said tasks being different from the execution of others of said tasks ([0008]),

and wherein each of said plurality of computers is dedicated to communicate with at least three of said plurality of computers within said matrix ([0072]), and each of the plurality of computers includes read-only memory for storing data and instructions, random access memory for storing data and instructions, and a processor for executing the instructions (Schreiber col 32 lines 1-24).

50. Claims 5, 22, 29, 35, 36, 43, 44 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii/Pechanek1/Schreiber in view of Common Art (asynchronous communication).

51. Regarding claim 5, Fujii/Pechanek1 discloses the computer array of claim 1, but fails to disclose that the communication between the computers is asynchronous.

Examiner takes Official Notice that asynchronous communication is common in the art.

Fujii/Pechanek1/Scheiber would have been motivated to utilize the asynchronous communication in order to speed up reaction time (rather than waiting for a clock) and to make a universal clock signal unnecessary.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system of Fujii/Pechanek1 and incorporate the asynchronous communication found in Common Art.

52. Claims 22, 29, 35, and 44 are rejected under the same grounds as claim 5.

53. Regarding claim 36, Fujii.Pechanek1/Scheiber discloses the computer array of claim 35, wherein: each of the computers includes dedicated memory [0050].

54. Regarding claim 43, Fujii/Pechanek1/Scheiber discloses a computer array, comprising: a plurality of computers on a unitary substrate (Pechanek1 col 2 lines 25-27) operating asynchronously (Common Art); and a plurality of data paths between the computers, each of the data paths facilitating communication between some, but not all, of the computers (fig. 11); and wherein at least some of the computers are assigned a task different from that assigned to the other computers ([0008]).

55. Regarding claim 56, Fujii/Pechanek1/Scheiber discloses a computer array, comprising: at least twenty-four computers (fig. 5) integrated in a unitary substrate (Pechanek1 col 2 lines 25-27); and a plurality of data paths connecting the computers, the data paths being dedicated for communication between associated pairs of the computers ([0072]), and werein, each of the computers is coupled to communicate with at least to other computers (fig. 11); each of the computers operates internally in an asynchronous manner (Common Art); each of the computers communicates with the other computers asynchronously (Common Art); and each of the computers has dedicated memory ([0050])

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii/Pechanek1/Schreiber in view of Common Art (flash memory).

56. Regarding claim 15, Fujii/Pechanek1/Schreiber discloses the method of claim 14, but fail to disclose that at least one of the computers communicates with flash memory.

The addition of Schreiber has included a ROM and Examiner takes Official Notice that a typical type of ROM is flash memory.

Fujii/Pechanek1/Schreiber contains instruction memory, data memory, and register memory (among others) for successful operation. The combination would have been motivated to utilize flash memory among its memory requirements because it is nonvolatile, contains no moving parts, is silent, and has a very fast access time.

It would have been obvious at the time of the invention for one of ordinary skill in the art to take the processing system ROM of Fujii/Pechanek1/Scheiber and incorporate the flash memory of Common Art.

57. Claims 31 and 33 are rejected under the same grounds as claim 16.

Response to Arguments

58. Many of Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. Arguments still relevant are presented below.

59. Applicant asserts that Fujii's array-type processor with a plurality of processor elements cannot be characterized as an array of processors, where each element is characterized as a processor. Examiner disagrees. Array-type processors are commonly characterized in both ways and each is reasonable. Consider, for example, Schreiber col 32 lines 1-24, which characterizes the elements as separate processors.

60. Applicant argues that Fujii's communication lines are not dedicated because there is a switching mechanism that alters the connectivity. Examiner disagrees. The lines, as clearly shown in Fujii Fig. 2 are clearly dedicated. Indeed, the use of an input multiplexer does not change this. In fact, Examiner would be interested to know how Applicant intends to handle multiple processor element inputs without the use of some type of multiplexer, as Applicant's specification provides little disclosure in this regard.

61. Applicant objects to the Official Notice of the asynchronous system. The following reference has been provided: Schmidt (U.S. Patent No. 5,410,723).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian P Johnson whose telephone number is (571) 272-2678. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Brian Johnson/ Patent Examiner, Art Unit 2183

/Eddie P Chan/

Supervisory Patent Examiner, Art Unit 2183